Fully Resonant Adaptive Gate Driver Scheme for GaN Mosfets

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# Introduction

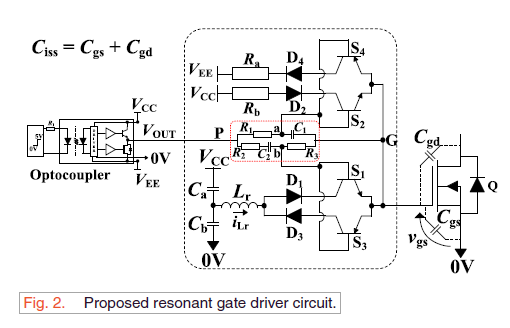
Resonant Gate Driver schemes were studied and a new scheme for a fully resonant gate driver is proposed. This document summarises the problems in existing topologies as well as issues that one might face while developing this new scheme further.

# Literature Review

The primary paper studied is

J. V. P. S. Chennu, R. Maheshwari and H. Li, "New Resonant Gate Driver Circuit for High-Frequency Application of Silicon Carbide MOSFETs," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8277-8287, Oct. 2017.

URL: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7869365&isnumber=8031005>



Issues:

1. Ra and Rb are selected arbitrarily (to limit gate current).
2. The importance of D2 and D4 (for blocking reverse current through BJT) barring exceptional circumstances.
3. Vee acts as a sink and must be bidirectional. The nature of this voltage source has not been addressed.
4. The values of Ca and Cb are not chosen according to the steady state equation given in section F4.

# Value of Ra and Rb

The value of resistances is determined by the maximum gate current allowed in the gate path which in turn is limited by the maximum collector current rating of the small signal transistor.

At the same time, the maximum allowed gate current for a Mosfet needs to be analysed. While manufacturers like Infineon and Panasonic mention the maximum peak pulsed gate current rating and the maximum average gate current rating in their datasheet, other manufacturers like cree and GaNSystems do not mention these ratings. This parity needs to be analysed further.

As of now, we must try to make the switching conditions similar to the test switching circuit given in the datasheet.

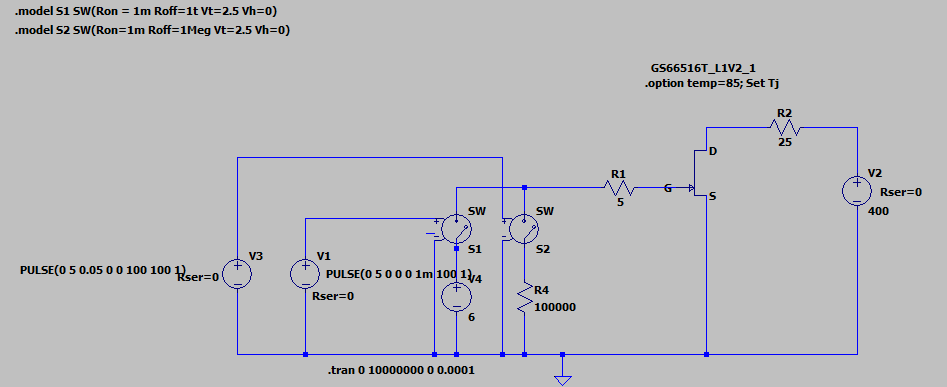
# D2 and D4

While they might not be required during normal operation as there is no overshoot on either voltage extreme, they are a necessary component to increase reliability. In cases of high dV/dt in Vds, there is overshoot in Vgs which will lead to reverse current flowing through the transistors.

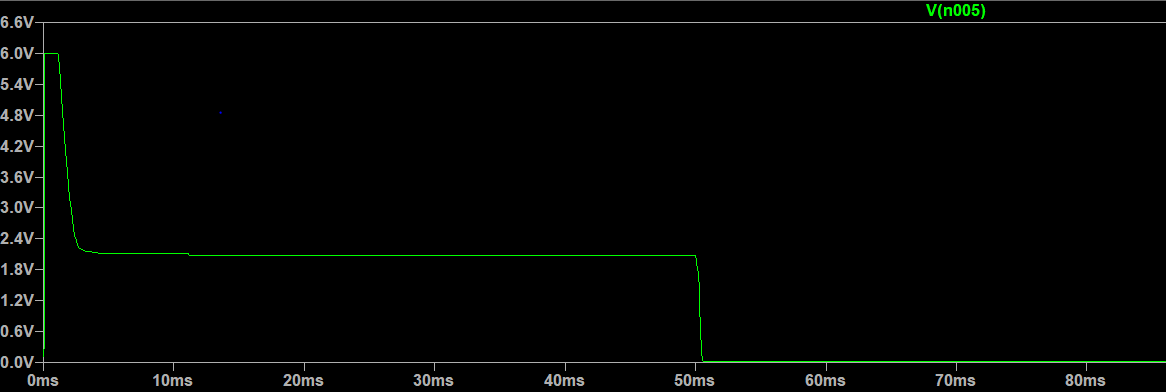
MOSFETs may be used in place of BJT and diodes to have clamping capability irrespective of the nature of gate voltage. This will lead to a more complex drive circuit which needs to be analysed further.

# Study of floating gate

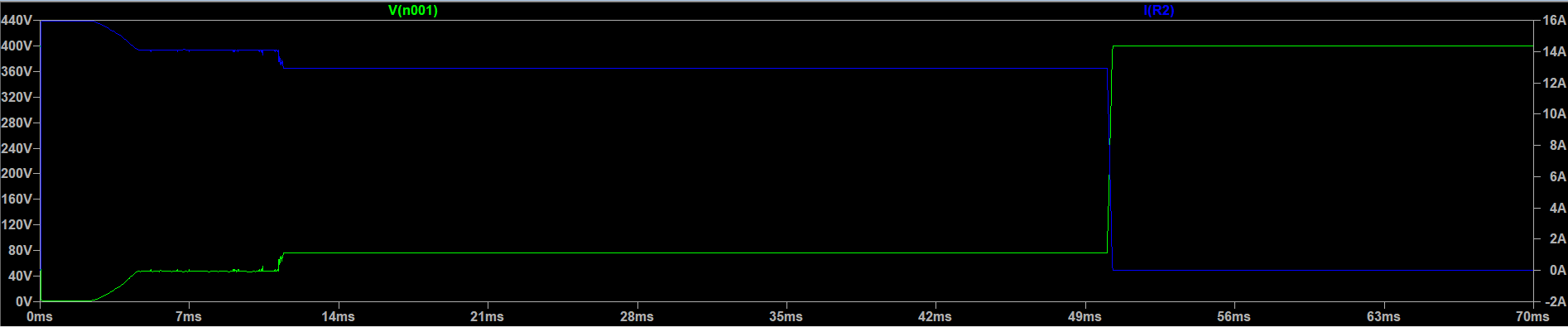
LTSpice Simulations



Vgs:



Vds and Ids:



Problems: Why does Vds suddenly jump from 40V to 70 V and then stabilises?

Conclusions:

The gate, if left floating after rise time, should work fine during normal switching operation at high frequency. But it is not recommended as it decreases reliability and may lead to false switching due to transients in other parts of the circuit.

# Block diagram of proposed scheme

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Overall detailed analysis of which converters to be used, bjt/mosfet driving circuit, control strategies needs to be done.